This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended): A system suitable for providing a search, comprising:
a central controller suitable for implementing search and edit operations; and
at least one search engine communicatively coupled to the central controller,
wherein the central controller performs parallel execution of a search operation and an edit operation through utilization of a binary search tree and the at least one search engine.

2. (original): The system as described in claim 1, wherein the central controller and at least one engine are communicatively coupled via a search connection, an edit connection and a cache connection.

3. (original): The system as described in claim 1, wherein the at least one search engine includes a priority controller, memory, edit module, search module and address cache.

4. (original): The system as described in claim 3, wherein the priority controller manages access to the memory by the edit module, search module and cache module.

5. (original): The system as described in claim 3, wherein the priority controller accesses data utilizing the address cache, the address cached configured to the address cached configured to receive data from the memory.

6. (original): The system as described in claim 3, wherein the edit module connects with the memory through the priority controller, the edit module configured to perform calculations for editing operations.

7. (original): The system as described in claim 3, wherein the search module is configured to perform calculation for a search operation.

8. (original): The system as described in claim 7, wherein the search module is communicatively connected to a second search module of a second search engine positioned at a neighboring level, the second search engine positioned at least one of at a previous or subsequent level to the search module.

9. (original): The system as described in claim 7, wherein the search engine is a 0th level search engine, output of the search module is provided to the central controller and wherein the search engine is a top search engine, the input of the search module is obtained from the central controller.

10. (original): The system as described in claim 3, wherein the edit module has inputs and outputs from a neighboring search engine level to the search engine.

11. (original): The system as described in claim 3, wherein the priority controller gives priority to a search operation over an edit operation.

12. (original): The system as described in claim 3, wherein the priority controller accesses the address cache to provide parallel access.

13. (original): The system as described in claim 12, wherein the priority controller receives a request to read a memory address of the memory, content of the memory address is copied to a first cache address and a second cache address of the address cache.

14. (currently amended): A search engine suitable for providing a search, comprising:

a memory suitable for storing electronic data;

a priority controller communicatively coupled to the memory;

an edit module communicatively coupled to the priority controller, the edit module configured to perform calculations for an edit operation;

a search module communicatively coupled to the priority controller, the search module configured to perform calculations for a search operation; and

an address cache communicatively coupled to the memory and the priority controller, the address cache suitable for storing electronic data;

wherein the priority controller manages access to the memory by the edit module, search module and address cache, and the search engine provides the search using a binary search tree.

15. (original): The search engine as described in claim 14, wherein the priority controller, through utilization of the address cache enables parallel execution of a search operation and an edit operation as performed by the search module and edit module respectively.

16. (original): The search engine as described in claim 14, wherein the search module is communicatively connected to a second search module of a second search engine position at a neighboring level, the second search engine positioned at least one of at a previous or subsequent level to the search module.

17. (original): The search engine as described in claim 14, wherein the edit module has inputs and outputs from a neighboring search engine level to the search engine.

18. (original): The search engine as described in claim 14, wherein the priority controller gives priority to a search operation over an edit operation.

19. (original): The search engine as described in claim 14, wherein the priority controller accesses the address cache to provide parallel access.

20. (original): The search engine as described in claim 19, wherein the priority controller receives a request to read a memory address of the memory, content of the memory address is copied to a first cache address and a second cache address of the address cache.

21. (currently amended): A system suitable for providing a search, comprising:

a central controller suitable for implementing search and edit operations, the central controller suitable from inputting and outputting external communications; and

a plurality of search engines arranged in zero through *k* levels, wherein *k* level search engine of the plurality of search engines is communicatively coupled to the central controller and a zero level search engine of the plurality of search engines is communicatively coupled to the central controller, wherein the central controller performs parallel execution of a search operation and an edit operation through utilization of a binary search tree and at least one of the plurality of search engines.

22. (original): The system as described in claim 21, wherein the central controller and the plurality of search engines are communicatively coupled via a search connection, an edit connection and a cache connection.

23. (original): The system as described in claim 21, wherein at least one of the search engines include a priority controller, memory, edit module, search module and address cache.

24. (original): The system as described in claim 23, wherein the priority controller manages access to the memory by the edit module, search module and cache module.

25. (original): The system as described in claim 23, wherein the priority

controller accesses data utilizing the address cache, the address cached configured to receive data from the memory.

26. (original): The system as described in claim 23, wherein the edit module connects with the memory through the priority controller, the edit module configured to perform calculations for editing operations and wherein the search module is configured to perform calculation for a search operation.

27. (original): The system as described in claim 26, wherein the search module is communicatively connected to a second search module of a second search engine position at a neighboring level, the second search engine positioned at least one of at a previous or subsequent level to the search module.

28. (original): The system as described in claim 27, wherein the search engine is included in the zero level search engine, output of the search module is provided to the central controller and wherein the search engine is included in the *k* level search engine, the input of the search module is obtained from the central controller.

29. (original): The system as described in claim 23, wherein the edit module has inputs and outputs from a neighboring search engine level to the s earch engine.

30. (original): The system as described in claim 23, wherein the priority controller gives priority to a search operation over an edit operation.

31. (original): The system as described in claim 23, wherein the priority controller accesses the address cache to provide parallel access.

32. (original): The system as described in claim 31, wherein the priority controller receives a request to read a memory address of the memory, content

of the memory address is copied to a first cache address and a second cache address of the address cache.